DELTA – SIGMA MODULATORS WITH IMPROVED NOISE PERFORMANCE

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates in general to switched-capacitor techniques and in particular to delta – sigma modulators with improved noise performance.

DESCRIPTION OF THE RELATED ART

[0002] Delta-sigma modulators are particularly useful in digital to analog and analog to digital converters (DACs and ADCs). Using oversampling, the delta-sigma modulator spreads the quantization noise power across the oversampling frequency band, which is typically much greater than the input signal bandwidth. Additionally, the delta sigma modulator performs noise shaping by acting as a lowpass filter to the input signal and a highpass filter to the noise; most of the quantization noise power is thereby shifted out of the signal band.

[0003] The typical delta sigma modulator includes a summer summing the input signal with negative feedback, a linear filter, quantizer and a feedback loop with a digital to analog converter coupling the quantizer output and the inverting input of the summer. In a first order modulator, the linear filter comprises a single integrator stage while the filter in a higher order modulator comprises a cascade of a corresponding number of integrator stages. The quantizer can be either a

one-bit or a multiple-bit quantizer. Higher-order modulators have improved quantization noise transfer characteristics over those of lower order, but stability becomes a more critical design factor as the order increases.

[0004] Switched-capacitor filters / integrators are useful in a number of applications including the integrator stages in delta sigma modulators. Generally, a basic differential switched-capacitor integrator samples the input signal onto sampling capacitors during the sampling (charging) phase. A reference voltage may also be sampled onto a reference sampling capacitors during this phase. During the following dump phase, the charge on the sampling capacitor is transferred at the summing node of an operational amplifier to the integrator capacitor in the amplifier feedback loop. The operational amplifier drives the integrator output.

[0005] Noise performance is an important design constraint in delta-sigma modulator development. Noise can result from a number of different factors, including parasitic capacitances and timing mismatches. Hence, for applications requiring low-noise delta-sigma modulation, improved techniques for reducing noise are required.

SUMMARY OF THE INVENTION

[0006] Circuits and methods according to the inventive principles are particularly useful in improving the performance of delta sigma modulators, such as those used in digital to analog and analog to digital converters. a corresponding capacitor during a sampling phase. According to one particular embodiment, an integrator stage is disclosed for use in a delta sigma modulator

includes an operational amplifier, an integration capacitor coupling an output of the operational amplifier and a summing node at an input of the operational amplifier, and a feedback path. The feedback path includes first and second capacitors having first plates coupled electrically in common at a common plate node and switching circuitry for sampling selected reference voltages onto second plates of the capacitors during a sampling phase. The integrator stage further includes a switch for selectively coupling the common plate node and the summing node during an integration phase.

[0007] Among the many advantages afforded by the application of the inventive concepts are improved noise performance and a relaxation in the design constraints on the modulator integrator stages. By isolating the reference path feedback switches from the summing nodes during sampling, non-linearities caused by parasitic capacitances of those switches can be avoided. Additionally, techniques are disclosed for implementing signal energy cancellation within the delta-sigma loop thereby reducing the in-loop noise to small amounts of quantization noise.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] FIGURE 1 is a high level functional block diagram of an analog to digital converter suitable for illustrating the application of the inventive principles;

[0010] FIGURE 2 is a functional block diagram of an exemplary 5th order delta-sigma modulator suitable for use in circuits and systems such as the analog to digital converter shown in FIGURE 1;

[0011] FIGURE 3A is a more detailed functional block diagram of the first integrator stage and integral multiple-bit DAC shown in FIGURE 2;

[0012] FIGURE 3B is a more detailed functional block diagram of the integral multiple-bit DAC shown in FIGURE 3A;

[0013] FIGURE 3C is a conceptual diagram of one of the switches of FIGURE 3B showing representative parasitic capacitances; and

[0014] FIGURE 4 is a timing diagram illustrating the operation of the delta-sigma modulator of FIGURE 2.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The principles of the present invention and their advantages are best understood by referring to the illustrated embodiment depicted in FIGURE 1-4 of the drawings in which like numbers designate like parts.

[0016] FIGURE 1 is a high-level functional block diagram of a single-chip audio analog-to-digital (A/D) 100 suitable for practicing the principles of the present invention. A/D converter 100 is only one of a number of possible applications employing delta-sigma data converters. Other examples include digital to analog converters (DACs) and Codecs.

[0017] A/D converter 100 includes two conversion paths for converting left and right channel analog audio data respectively received at left and right analog differential inputs AINL+/- and AINR+/-. The analog inputs are each passed through an input gain stage 101a – 101b and then to a delta – sigma analog to a digital converter (ADC) 200a – 200b, which will be described in detail in conjunction with FIGURE 2. The digital outputs of delta-sigma ADCs 200a – 200b are passed through a decimation filter 107, which reduces the sample rate, and a low pass filter 108. Delta sigma ADCs 200a – 200b sample the analog signal at the oversampling rate and output digital data, in either single-bit or multiple-bit form depending on the quantization, at the oversampling rate. The resulting quantization noise is shaped and generally shifted to frequencies above the audio band.

[0018] The resulting left and right channel digital audio data are output through a single serial port SDOUT of serial output interface 109, timed with serial clock SCLK and left-right clock LRCLK in accordance with the Digital

Interface Format (DIF). The SCLK and LRCLK clocks can be generated externally and input to converter 100 or can be generated on-chip, along with the associated data, in response to a received master clock MCLK.

[0019] FIGURE 2 is an exemplary 5th order delta-sigma modulator 200 comprising an input summer 201 and five (5) integrator stages 202a - 202e. Delta sigma modulator 200 is a weighted feed-forward design in which the outputs of each of the integrator stages are passed through a gain stage (amplifier) 203a-203e to an output summer 204. Amplifiers 203a – 203e allow the outputs of the integrator stages to be weighted at the summer 204 input. The output from summer 204 is quantized by a multiple-bit quantizer 205, which generates the multiple-bit digital output signal. Additionally, the output from quantizer 205 is fedback to the inverting input of summer 201 through dynamic element matching (DEM) circuitry 206 and multiple-bit digital to analog converter (DAC) 207. (A 5th order feed-forward design was selected for discussion purposes; in actual implementation; the order as well as the configuration of the modulator will vary. A general discussion of delta-sigma modulator topologies can be found in the literature, for example, in Norsworthy et al., *Delta-Sigma Data Converters, Theory, Design and Simulation,* IEEE Press, 1996).

[0020] FIGURE 2 also shows an additional feed-forward path, including amplifier 208, between modulator input 210 and summer 204. The gain of amplifier stage 208 is preferably:

Gain = (1/Quantizer gain) * (1/Multi-Bit DAC gain)

The purpose of this additional feed-forward path is to cancel as much of the input signal energy from the delta-sigma loop as possible. Consequently, most of the noise within the modulator will be quantization noise. In turn, the design

constraints on the sub-circuits within modulator 200 can be relaxed. For example, the first integrator stage 202a is typically the major contributor to the noise performance of the entire modulator. This feed-forward technique results in less signal energy at the output of the first integrator stage and hence such parameters as the stage opamp DC gain can be reduced. In turn, the power consumption of the device as well as the die size can be reduced.

[0021] FIGURE 3A is an electrical schematic diagram of an integral switched-capacitor summer – DAC – integrator circuit 300 corresponding to first integrator stage 202a, summer 204 and DAC 207 of delta sigma modulator 200. Generally, the design of the first integrator stage of a delta- sigma modulator is the most critical to setting the distortion performance and therefore will be the focus of the following discussion. However the concepts discussed below are useful in a number of switched capacitor applications, including various delayed and undelayed switched capacitor integrators.

[0022] Switched capacitor integrator 300 generally operates in two non-overlapping Phases ϕ_1 and ϕ_2. The timing of Phases ϕ_1 and ϕ_2 is shown in FIGURE 4. Delayed Phases ϕ_{1d} and ϕ_{2d} are delayed versions of Phases ϕ_1 and ϕ_2. As will be discussed further, in the preferred embodiment each delayed phase is composed of rough (R) and fine (F) subphases (Subphases ϕ_{1dR}, ϕ_{1dF}, ϕ_{2dR}, ϕ_{2dF}). Additionally, in the illustrated embodiment, a double sampling technique is utilized to sample the input signal V_{IN} and/or the reference signal V_{REF}. For double sampling, the input plate of the each sampling capacitor is coupled to either V_{IN} or V_{REF} during ϕ_1 sampling with a given polarity. During ϕ_2 integration, the charge on each sampling capacitor input plate is then forced to

the opposite plate by reversing the polarity of the corresponding voltage at that input plate.

[0023] In the general case, switches 304a-304b close during Phase ϕ_1. During Delayed Phase ϕ_{1d} switches 301a-301d and 304a- 304b close and the differential input voltage V_{IN} is sampled onto input sampling capacitors (C_{IN}) 303a-303b. Switches 302a-302d and 305a-305b are open during Phase ϕ_1.

[0024] Also during Phase ϕ_1 the reference voltage is sampled by DAC 207 for presentation to summing nodes A and B. Two data paths of an n-bit DAC operating in response to digital bits and their complements (D and /D) from DEM circuitry 206 are shown in further detail FIGURE 3B for reference.

[0025] Generally during Phase ϕ_1, the differential reference signal V_{REF} is sampled onto reference sampling capacitors (C_{REF}) 306a-306b for each path by switches 307a-307d and 304a-304b (FIGURE 3A). Switches 309a-309d (FIGURE 3A) are open during Phase ϕ_1. Switches 310a-310d for each path, under the control of complementary bits Dx and /Dx, couple or cross-couple the input plates of reference sampling capacitors C_{REF} 306a-306b to the common plate (charge sharing) nodes A and B (where x is the index for the corresponding bit / reference sampling path from 0 to n from the quantizer and DEM circuitry). In other words, the configuration of switches 310a-310d for a given reference sampling path sets the polarity of the voltage at the input plates of capacitors 306a-306b.

[0026] During Phase ϕ_2 the sampling switches reverse their configuration with switches 302a-302d closing and switches 301a-301d and 304a-304d opening for the input signal path. For the reference path, switches 307a-307d

open and switches 309a-309d close. The charge on the input plates of capacitors C_{IN} and C_{REF} is forced to the output (top) plates and common plate (charge sharing) nodes A and B. During Delayed Phase ϕ_{2d} switches 305a-305b close to transfer the charge at common nodes A and B from the top plates of reference sampling capacitors C_{IN} and C_{REF} to the the summing nodes at the inverting (-) and non-inverting (+) inputs of opamp 312 (the summing nodes) and integrator capacitors (C_I) 313a-313b.

[0027] As previously noted, the preferred integrator 300 operates in rough and fine subphases. During Rough Delayed Subphase ϕ_{1dR}, the input plates of sampling capacitors C_{IN} and C_{REF} are driven by rough buffers 314a-314d and 315a-315d which provide an increased charging current. Subsequently, input plates P are brought to their full sampling voltage during Delayed Fine Subphase ϕ_{1dF} by direct coupling to the corresponding input or reference voltage. More importantly, rough buffers 314 and 315 provide increased drive during Rough Delayed Subphase ϕ_{2dR} to rapidly slew the voltage on capacitor input plates P towards the opposite voltage to transfer the sampled charge to the top plates P' and integration capacitors C_I. The charge transfer is completed during Delayed Fine Subphase ϕ_{2dF} by direct coupling of the input and reference capacitor (C_{IN} and C_{REF}) input plates P to the appropriate input.

[0028] According to the inventive concepts, DAC switches 310 are disposed in front of reference capacitor 306 of each reference path. In other words, switch 310 switches the charge at the input plates P of capacitors C_{REF}. This is in contrast to conventional designs in which the charge summing is done at output or top plates P'.

[0029] With switches 310 disposed in front of reference capacitors C_{REF}, the top plates of corresponding reference capacitors 306a and 306b is preferably either fabricated in common or tied together. This feature is shown generally in FIGURE 3B by lines 311a – 311b represent the commonality of all top plates P' of reference capacitors 306a (lines 311a) and the commonality of all top plates P' of reference capacitors 306b (lines 311b).

[0030] FIGURE 3C is a conceptual schematic diagram of one switch 310 illustrating the gate – source parasitic capacitance C_{GS} and the gate – drain parasitic capacitance C_{GD}. Control signals Dx and /Dx, coming from the quantizer 205 and DEM 206 circuitry, are independent of the modulator input signal. Hence, when switches 310 turn on and off, parasitic capacitances C_{GS} and C_{GD} charge and discharge independent of the input signal. If this charge were to be coupled into the integration capacitors C_I, non-linearities would appear in the opamp 312 output and consequently in the entire system in general. With the configuration of FIGURE 3B however, switches 310 are isolated from the summing nodes A and B such that non-linearities are not introduced by the parasitic capacitances of switches 310.

[0031] The configuration of switches 310 by control signals Dx and /Dx is set before the start of the current ϕ_1. In order for this "decision" to be made in sufficient time, control signals Dx and /Dx are preferably generated during ϕ_2 of the prior cycle. This timing allows Dx and /Dx to propagate from the quantizer 206 outputs and through DEM circuitry 207 to switches 310 before the rising edge of Phase ϕ_1 of the current cycle.

[0032] One advantage of the configuration of FIGURE 3B is its ability to cancel charge at the common plate (charge sharing) nodes A and B. In an ideal

delta- sigma modulator the input signal charge and feedback charge at nodes A and B cancel such that only a small quantization noise charge is transferred onto integration capacitors C_I. In actual practice however, if the two charges do not reach the summing nodes at or approximately the same time, then a large input signal or feedback signal charge will be transferred onto the integration capacitors. If this event occurs, a large signal swing will appear at the opamp outputs.

[0033] In contrast to conventional modulator topologies, in modulator 200 the input signal and feedback charges are summed at common nodes A and B, which are disposed in front of summing switches 305. Consequently, during ϕ_1 the charges from the input and reference capacitors and C_{IN} and C_{REF} are shared at Nodes A and B before summing switches 305 close and the charge is transfered to the summing nodes at the operational amplifier inputs. As indicated above, during Phase ϕ_2 the charge from all paths are switched to charge sharing nodes A and B. This timing allows input and feedback charge from capacitors C_{IN} and C_{REF} to cancel at nodes A and B such that only a small quantization noise charge is transferred to the opamp inputs during Phase 2 delayed (ϕ_{2d}) when switches 305 close.

[0034] Preferably, nodes A and B for the first integrator stage are disconnected from the signal inputs V_{IN+} and V_{IN-} prior to disconnection of the signal feed-forward path. Moreover, the input signal feedforward path is preferably disconnected from the modulator inputs shortly after the quantizer comparison operation. The advantage of taking these steps is the minimization of unwanted sampling of signals caused by descriptions of the feedforward path. Additionally, the feedforward path provides a possible link between the input

signal and internal quantization noise. Hence attention must be paid to the design of the feedforward path to avoid possible dilution of the input signal.

[0035] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.